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To cite this article: Hong-Kyu Seo *et al* 2017 *2D Mater.* **4** 024001

2D Materials

PAPER

RECEIVED
7 October 2016

REVISED
6 December 2016

ACCEPTED FOR PUBLICATION
15 December 2016

PUBLISHED
11 January 2017

Direct growth of graphene-dielectric bi-layer structure on device substrates from Si-based polymer

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Keywords: graphene, solid carbon source, graphene-dielectric bi-layer, polydimethylsiloxane, organic field-effect transistor

Supplementary material for this article is available online

Abstract

To facilitate the utilization of graphene films in conventional semiconducting devices (e.g. transistors and memories) which includes an insulating layer such as gate dielectric, facile synthesis of bi-layers composed of a graphene film and an insulating layer by one-step thermal conversion will be very important. We demonstrate a simple, inexpensive, scalable and patternable process to synthesize graphene-dielectric bi-layer films from solution-processed polydimethylsiloxane (PDMS) under a Ni capping layer. This method fabricates graphene-dielectric bi-layer structure simultaneously directly on substrate by thermal conversion of PDMS without using additional graphene transfer and patterning process or formation of an expensive dielectric layer, which makes the device fabrication process much easier. The graphene-dielectric bi-layer on a conducting substrate was used in bottom-contact pentacene field-effect transistors that showed ohmic contact and small hysteresis. Our new method will provide a way to fabricate flexible electronic devices simply and inexpensively.

1. Introduction

Due to the outstanding electrical properties of graphene, various methods have been developed to synthesize graphene for use in electronic devices [1–9]. Currently, the most promising way to synthesize large-area and highly-functional graphene is chemical vapor deposition (CVD) using CH_4 or C_2H_2 gas on catalytic metal [4, 10–12]. However, CVD is dangerous because CH_4 and C_2H_2 are explosive, and inconvenient because it requires an additional transfer process to move the graphene to the target substrates. To overcome these obstacles, a graphene synthesis method that uses a solid carbon source and that grows graphene directly on substrate has been developed [13–17]. This method is simple, safe, scalable and inexpensive because it uses solution-processable cheap carbon source that can be spin-coated over a large area. Even with this method, to utilize the graphene films in conventional semiconducting devices, insulating layers such as a gate dielectric in thin film transistors are required. However, the separate formation of a dielectric layer in contact with a graphene layer is usually complicated and expensive to prepare [18, 19].

Until now, the graphene growth methods have focused on the synthesis of graphene itself so that the development of a new method that can synthesize bi-layers composed of a graphene film and a dielectric layer simultaneously is of prime importance from the perspective of sustainable industrial mass production. One of the most promising materials as a precursor for the synthesis of graphene-dielectric bi-layer (GDB) structure is polydimethylsiloxane (PDMS). PDMS is a cheap carbon source for graphene growth, and it is also a widely-used gate dielectric material in field-effect transistors (FETs) [20–24]. Unlike the oxide dielectric layer, it forms a nonpolar elastomer dielectric layer that is free from carrier trapping that causes pronounced hysteresis and shift of threshold voltage under repeated and bidirectional operation [22, 25–27]. Furthermore the elasticity and flexibility of the PDMS dielectric layer can be exploited in flexible FETs or pressure sensors [23, 24]. Therefore, discovery of a way to synthesize GDB structure for electronic devices by simple process

would be a significant advance in synthesis and applications of graphene.

Here we introduce a one-step conversion method to grow a GDB structure directly on electronic device substrates from solution-processed PDMS. Spin-coating of PDMS solution can provide a flat and uniform precursor film with controllable thickness over a large area on a substrate. PDMS on a Si wafer substrate was annealed under high temperature, with a Ni layer deposited on the PDMS as a metal catalyst for graphene growth. High-quality multi-layer graphene (MLG) was formed at the interface between PDMS and Ni layer, thereby leaving the annealed PDMS (a-PDMS) layer on substrate. Therefore, we obtained GDB directly on a device substrate after removing the Ni capping layer, without additional graphene transfer or formation of a dielectric layer on substrate [13].

To demonstrate the practical application of this method, we fabricated bottom-contact organic FETs (OFETs) by using GDB (source/drain electrodes and gate dielectric) on a conductive substrate (gate electrode). OFETs based on graphene electrodes can take advantage of lower charge injection barrier between graphene electrodes and an organic channel than that between metal film electrodes and organic semiconductors [13, 28, 29]. Furthermore the materials except the substrate have excellent flexibility, so roll-to-roll processing fabrication of flexible OFETs is possible if the rigid substrate can replaced with a flexible one such as conductive metal foils.

2. Materials and methods

2.1. Fabrication and characterization of graphene-dielectric bi-layer films on substrate

PDMS solution (Si elastomer base, curing agent = 10:1 wt:wt SYLGARD 184, Dow Corning) as a precursor was spin-coated on Si wafer substrates (2 cm × 2 cm) at 5000 rpm for 5 min, then the samples were thermally cured on a hot plate for 1 h at 80 °C. Then, a 400 nm-thick Ni layer was deposited (Magnetron Sputtering System, SNTEK; working pressure 7 mTorr; power 50 W; Ar flow rate 50 sccm) on the PDMS layer as a metal catalyst for graphene growth. The samples were annealed using a vacuum furnace to synthesize GDB structure films at 800–1000 °C for 3 min with flowing 50 sccm Ar and 10 sccm H_2 at ~0.3 Torr. When the tube furnace temperature reached the set value, the furnace was moved to a sample zone that was kept at room temperature. After annealing, a cooling process was conducted with the same gas flow by moving the tube furnace away from the samples. The Ni layer was removed by dipping the samples into $FeCl_3$ metal etching solution (Iron(III) chloride solution 45°Be′, JUNSEI Chemical) for 30 min, and then rinsing with deionized water.

Characteristics of the resultant graphene were determined using Raman spectroscopy (WITEC Alpha 300R Raman spectroscope equipped with a 532 nm diode laser). Raman spectra were collected over a large area (50 μm × 50 μm, 2500 points) by Raman scanning. Sheet resistance R_S of graphene was measured using a four-point probe measurement system with a Keithley 2400 source measurement unit. Energy-dispersive spectrometry (EDS) spectra were measured using an EDS analyzer (XL30S FEG, Philips Electron Optics).

2.2. Fabrication and characterization of pentacene FETs.

Cross-sectional scanning electron microscope (SEM) images of PDMS and a-PDMS films were obtained using a high-resolution FE-SEM (JSM-7401F, JEOL). The capacitances of the PDMS and a-PDMS dielectric layers were measured using a precision LCR meter (HP4284A, Agilent Tech.). For capacitance measurement, the dielectric layers were located between the Si wafer substrate (2 cm × 2 cm) and the nine electrode pads (Ni, 400 nm, 1.3 mm × 2.3 mm). For FET fabrication, a patterned Ni layer (400 nm) that had a 100 μm gap was deposited on the PDMS layer through a shadow mask, and then samples were annealed at 900 °C for 3 min as described above. After Ni etching, the pentacene film (50 nm, Sigma-Aldrich) was deposited by organic molecular beam deposition (deposition rate = 0.1–0.2 Å s^{-1}, vacuum pressure = 10^{-6} Torr, substrate temperature = 25 °C) on MLG electrodes through a shadow mask. Electrical properties of FETs were characterized using a parameter analyzer (B1500A, Keysight).

3. Results and discussion

Graphene forms at the interface of the metal catalyst and the feedstock layer [13] so if the PDMS layer is thick enough, the remaining portion of the PDMS film forms an additional underlying layer that can be used as a dielectric layer. Therefore, we deposited the Ni layer as a catalyst and capping layer on a PDMS layer that was a few micrometers thick; this layer enables direct growth of GDB between the substrate and Ni layer. PDMS (4 μm)/Ni (400 nm) films on substrate were thermally annealed using vacuum furnace and formed a-PDMS/MLG/Ni/MLG structure (figure 1). At the interface between the PDMS layer and the Ni layer, the carbon atoms in PDMS surface diffused into the Ni layer under high temperature, and carbon atoms were released to form MLG on both sides of Ni layer during cooling [13–16, 30].

Raman analysis confirmed the formation of graphene films from the PDMS feedstock, and the optimal condition was established by evaluating the quality of graphene films (figure S1(a)) (stacks.iop.org/TDM/4/024001/mmedia) [13]. The samples were annealed at the optimal condition of 1000 °C for 3 min. In the average Raman spectrum (2500 points) of PDMS-derived graphene grown on the Ni layer (figure 2(a)), the ratio I_D/I_G of intensity I_D of the *D*

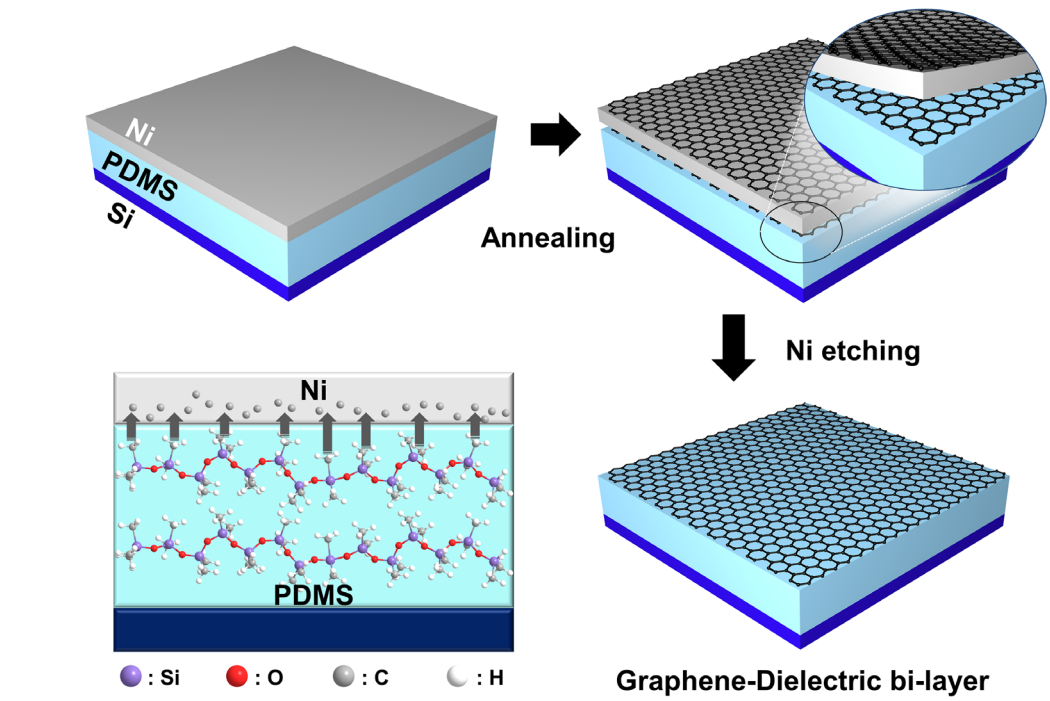

Figure 1. Schematic of synthesis procedure of graphene-dielectric bi-layer structure.

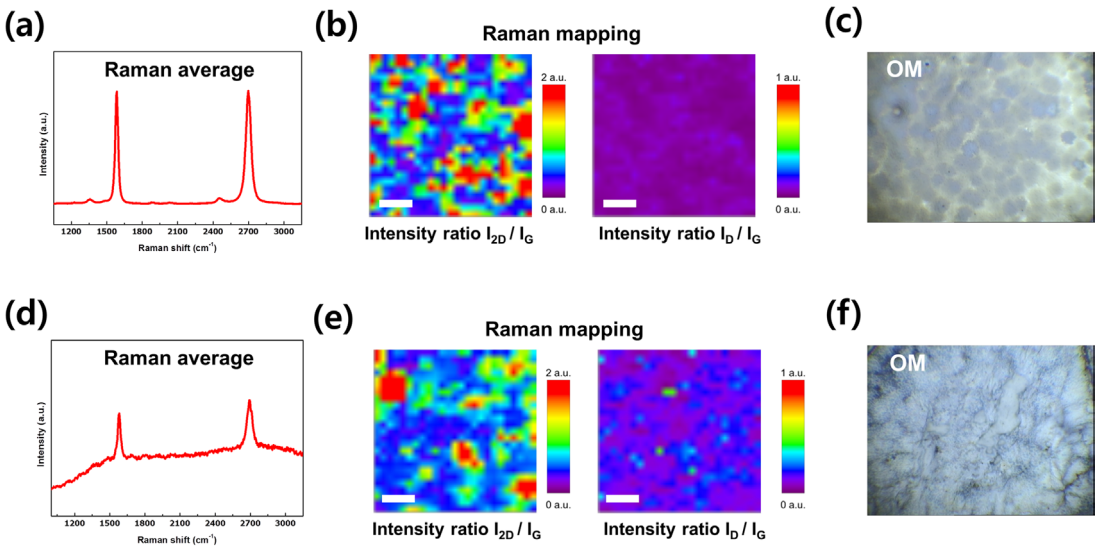

Figure 2. Average Raman spectrum (2500 points) of multi-layer graphene grown (a) on Ni layer and (d) under Ni layer. Raman mapping (50 μm × 50 μm) of *D*-to-*G* band peak intensity ratio I_D/I_G and 2D-to-*G* band peak intensity ratio I_{2D}/I_G in graphene grown (b) on Ni layer and (e) under Ni layer. Scale bar: 10 μm. Microscopy image of graphene grown (c) on Ni layer and (f) under Ni layer. Scale bar: 20 μm.

band (~1356 cm^{-1}) to the intensity I_G of the *G* band (~1585 cm^{-1}) was <0.1; this result indicates that the graphene film has few surface defects. Raman mapping of I_D/I_G over large area (50 μm × 50 μm) also showed high-quality of graphene (figure 2(b)). The formation of MLG was confirmed by optical images and Raman mapping of the ratio I_{2D}/I_G of the intensity I_{2D} of the 2D band (~2697 cm^{-1}) to I_G (figures 2(b) and (c)). MLG grown on the interface of the a-PDMS and the Ni layer at 1000 °C for 3 min was obtained directly on the a-PDMS layer after Ni had been removed by etching with $FeCl_3$. The MLG grown on Ni was removed with the Ni layer during Ni etching, and the underlying MLG remained on the a-PDMS layer (figure S2); this method enables direct growth of graphene on substrates, and avoids damage to graphene that can occur during a transfer process [13, 31]. In Raman analysis of MLG on the a-PDMS layer after Ni etching, average Raman spectrum with low $I_D/I_G < 0.1$ and Raman mapping of I_D/I_G means that high-quality MLG with few surface defects was also formed on the a-PDMS layer (figures 2(d) and (e)). From the Raman spectra of MLG at several points, we confirmed that the MLG is composition ranges from monolayers to a few layers (figure S1(b)).

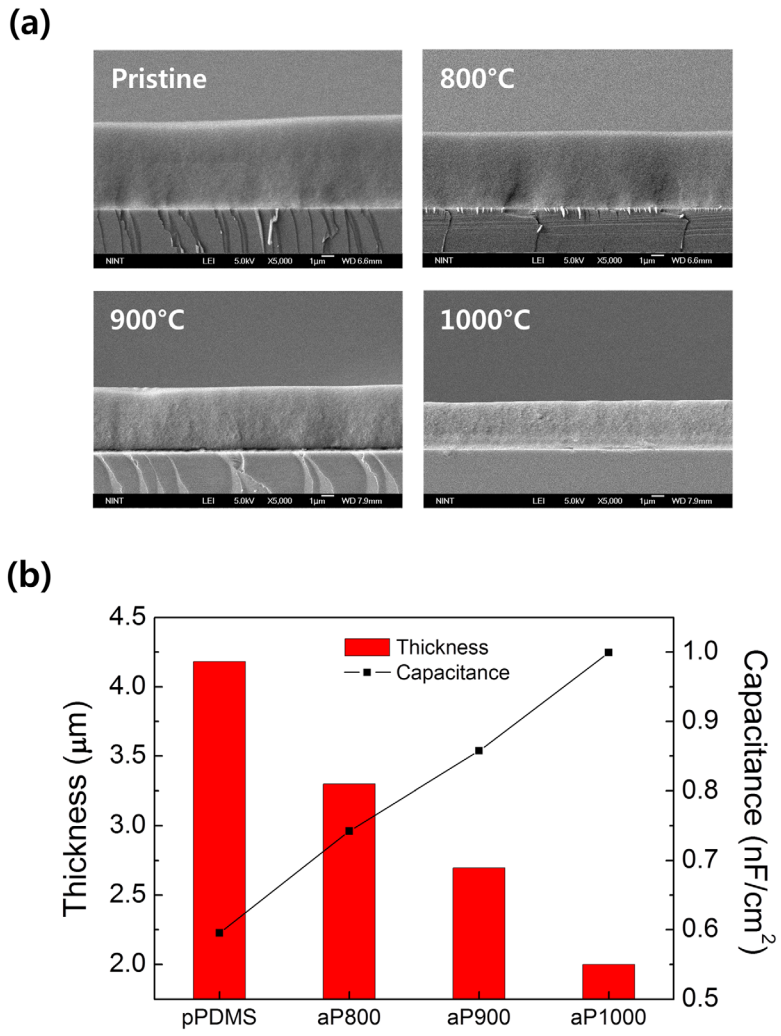

Figure 3. (a) Cross-sectional SEM images (×5000) of pristine PDMS and a-PDMS films annealed at 800, 900 and 1000 °C. Scale bar: 1 μm. (b) Change of film thickness and dielectric capacitance of PDMS films according to annealing temperature.

An optical image of MLG on a-PDMS layer showed different surface morphology than that of MLG on top of the Ni layer due to the different underlying layer (figure 2(f)). To verify complete etching of the Ni layer, we conducted an EDS analysis of each top layer before and after Ni etching [32–34]. A strong Ni peaks were detected before Ni etching (figure S3(a)), but no peaks related to Ni were detected after etching (figure S3(b)). These results mean that wet etching completely removed the Ni layer but left the MLG on the a-PDMS layer [13]. The MLG had very flat and uniform surface, and the MLG on a-PDMS layer had $R_S \sim 1.1$ kΩ sq^{-1}; the MLG grown at 800 and 900 °C for 3 min had $R_S \sim 5.8$ and ~1.6 kΩ sq^{-1}, respectively.

To confirm the successful formation of an insulating layer (a-PDMS) under the graphene layer, we used reactive ion etching (RIE) to remove MLG from the a-PDMS layer. RIE (O_2 gas, 100 W, 0.2 Torr) was applied several times per 10 s. R_S of MLG gradually increased during RIE, then lost its conductivity after 1 min; i.e. RIE removed MLG effectively. To utilize the a-PDMS layer as a dielectric for FETs based on graphene electrodes, the a-PDMS layer should have the similar dielectric constant (2.5–3.0) to that of pristine PDMS that has not been not annealed at high temperature [21–24]. Because the heat treatment results in a weight loss and shrinkage of the PDMS film, and could lead to internal damage of the film under some annealing conditions [35–38], we evaluated how change of annealing temperature affected the suitability of an a-PDMS layer as a dielectric for FETs. First, we prepared pristine PDMS (pPDMS) and a-PDMS films annealed at 800 (aP800), 900 (aP900) and 1000 °C (aP1000) for 3 min, and confirmed their film thickness by examining cross-sectional SEM images (figure 3(a)) and surface roughness by AFM analysis (table S1). The film thickness gradually decreased as annealing temperature increased, i.e. from ~4.2 μm for pPDMS to ~2.0 μm for aP1000. The dielectric capacitance of pPDMS, aP800, aP900 and aP1000 was measured, and the dielectric constant ε was calculated from the measured capacitance C as $\varepsilon = Cd/(\varepsilon_0 A)$ where d (m) is the thickness of dielectric layer, $\varepsilon_0 = 8.854 \times 10^{-12}$ F m^{-1}, and A (m^2) is the area of electrode (figure 3(b)) [39]. pPDMS, aP800 and aP900 had $2.6 \leqslant \varepsilon \leqslant 2.8$ which is comparable to the value reported previously [21–24]. However, the aP1000 had lower $2.2 \leqslant \varepsilon \leqslant 2.4$, and some of the area of evaporated Ni electrodes on aP1000 lost their dielectric

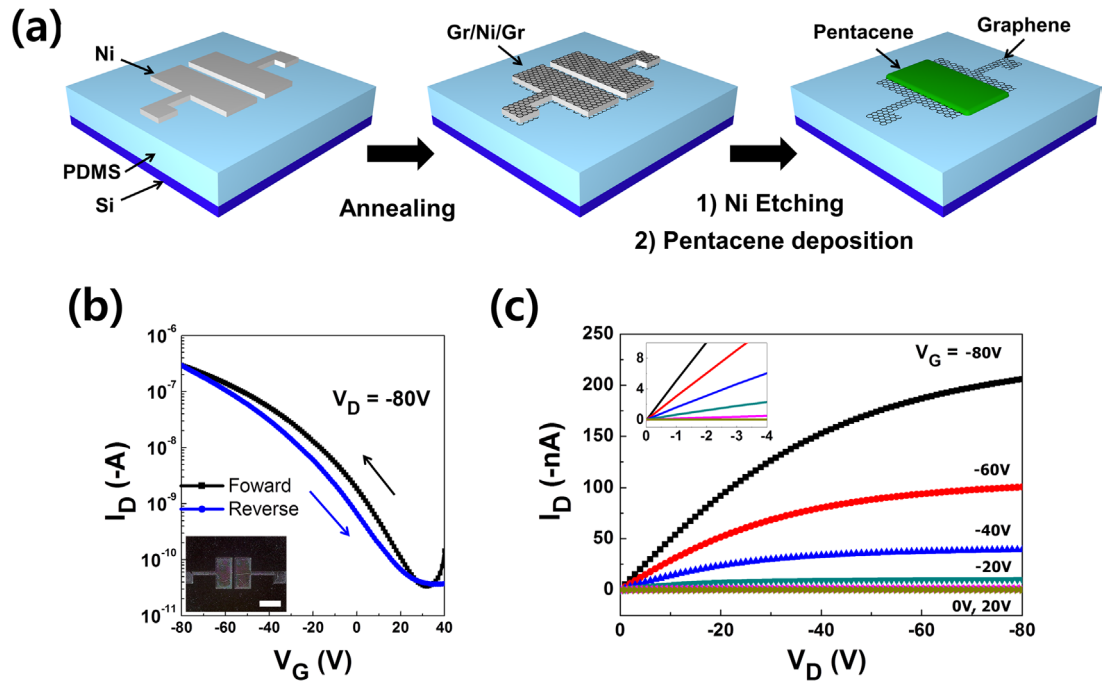

Figure 4. (a) Fabrication process of GDB based bottom-contact pentacene FETs (GP-FETs). (b) Transfer characteristics of GP-FETs (black: forward bias, blue: reverse bias). Inset: microscopy image of patterned source/drain graphene electrodes on a-PDMS. Scale bar: 1 mm. (c) Output characteristics of GP-FETs (channel length: 100 μm). Inset: output characteristics at low source-drain voltage.

property, possibly due to internal damage and structural transformation of the a-PDMS layer [35–38].

We fabricated bottom-contact OFETs to exploit our method (figure 4(a)). A patterned Ni layer was deposited on the PDMS layer through a shadow mask to obtain patterned graphene electrodes for OFETs. To optimize the combination of R_S and ε in the GDB structure; we annealed the layer at 900 °C for 3 min. After annealing, graphene films formed on areas that were covered by Ni. After Ni had been removed by etching, patterned source/drain graphene electrodes that had 100 μm gap were obtained directly on the a-PDMS layer (figure 4(b), inset). Finally, a 50 nm-thick pentacene layer was deposited on the graphene electrodes as an organic channel to finish OFET fabrication.

The electrical properties of bottom-contact pentacene FETs based on graphene electrodes and an a-PDMS dielectric layer (GP-FETs) were characterized by measuring their transfer and output characteristics. Their transfer curves showed typical p-type characteristic due to the pentacene channel (figure 4(b)). Calculated field-effect mobility μFET of GP-FET was ~0.01 $cm^2 \cdot V^{-1} \cdot s^{-1}$ in the saturation regime ($2L/W = 0.133$, $C_i = 0.86 \pm 0.01$ $nF \cdot cm^{-2}$), and GP-FETs showed on/off current ratio as high as 1.1×10^4 (at gate voltage $-80\,V \leqslant V_G \leqslant 30\,V$) that is suitable for switching active electronic devices. The device showed small hysteresis in forward and reverse scans; this characteristic means that the interface between the dielectric and the channel layer has a low density of deep traps that ensures the quality and consistency of the device [21, 22]. The output characteristic of GP-FETs showed clear gating effect and ohmic contact due to the low contact resistance and hole injection barriers between the graphene electrodes and the pentacene channel (figure 4(c)) [13, 28, 29]. We believe that our upcoming research could improve the performance of the OFETs through the reduction of PDMS thickness while considering graphene growth conditions, the formation of short channel length by introducing a photolithography, and the additional chemical treatment such as self-assembled monolayer (SAM) surface treatment.

4. Conclusion

We developed a facile, scalable, patternable, and inexpensive method that uses one-step thermal annealing of Si/PDMS/Ni to synthesize GDB from PDMS directly on device substrates. High-quality MLG films were grown on the top and bottom surfaces of the Ni layer, and MLG grown at the interface of the Ni and PDMS layer was obtained by removing the Ni by dipping the sample into $FeCl_3$. The top surface of PDMS was converted to MLG, but the remaining underlying a-PDMS layer has a dielectric property. Therefore, the graphene is easily patterned by deposition of patterned Ni layer on PDMS layer before annealing, so we fabricated bottom-contact pentacene FETs with MLG electrodes and a-PDMS dielectric layer. These GP-FETs showed ohmic contact between the graphene electrodes and the pentacene channel; due to the nonpolar a-PDMS dielectric layer they showed stable function with small hysteresis. Because this method to fabricate GDB uses only a solution process and thermal annealing, it is compatible with roll-to-roll

fabrication. This method is a promising way to fabricate conventional electronic devices using graphene layers as well as flexible electronic devices simply and inexpensively.

Acknowledgments

This work was supported by the Center for Advanced Soft-Electronics funded by the Ministry of Science, ICT and Future Planning as Global Frontier Project (CASE-2013M3A6A5073175), and the National Research Foundation of Korea(NRF) grant funded by the Korea government (Ministry of Science, ICT & Future Planning) (NRF-2016R1A3B1908431)

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